

## Preliminary Amendment

U.S. Patent Application Serial No. 09/321,605

forming an upper electrode of the capacitor on the oxide dielectric film;  
forming a second insulating film for covering the capacitor;  
forming a first opening for electrically connecting one of the couple of impurity diffusion layers and a second opening which exposes the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film;  
forming a metal film on the second insulating film for electrically connecting the one of the couple of impurity diffusion layers via the first opening and the upper electrode via the second opening;  
forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view, in a range which passes through the first opening and the second opening, by patterning the metal film;  
forming a third insulating film for covering the local interconnection;  
forming a third opening for electrically connecting to the other of the couple of impurity diffusion layers, by etching a part of the third insulating film; and  
forming a wiring electrically connecting to the other of the couple of impurity diffusion layers, the wiring composed from different material from the local interconnection.

21. (Thrice Amended) A method of manufacturing a semiconductor device comprising the steps of :  
forming a couple of impurity diffusion layers in a semiconductor substrate;

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forming a first insulating film covering the semiconductor substrate;  
forming a lower electrode of a capacitor on the first insulating film;  
forming an oxide dielectric film of the capacitor on the lower electrode;  
forming an upper electrode of the capacitor on the oxide dielectric film;  
forming a second insulating film for covering the capacitor;  
forming a first opening for electrically connecting one of the couple of impurity diffusion layers and a second opening which exposes the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film;  
*DZ*  
*and*  
forming a metal film on the second insulating film for electrically connecting the one of the couple of impurity diffusion layers via the first opening and the upper electrode via the second opening;  
forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view, in a range which passes through the first opening and the second opening, by patterning the metal film, wherein the local interconnection is a blocking layer for preventing a diffusion of a redundant to the oxide dielectric film;  
forming a third insulating film for covering the local interconnection;  
forming a third opening for electrically connecting to the other of the couple of impurity diffusion layers, by etching a part of the third insulating film; and  
forming a wiring electrically connecting to the other of the couple of impurity diffusion layers, the wiring composed from different material from the local interconnection.